## CLAIMS

1. A control unit for electronic microcontrollers or microprocessors that include a finite state machine having at least one combinatorial network, wherein the finite state machine comprises:

a plurality of control subunits, each control subunit corresponding to the at least one combinatorial logic network, each of the plurality of control subunits independently connected to an arbitration block to provide information about a possible future state and to receive a present state command.

2. The control unit according to claim 1 wherein each control subunit is structurally and functionally independent of the other control subunits.

3. The control unit according to claim 1 wherein each control subunit supplies the arbitration block with a predetermined value representing one of either a predetermined state of operation and a neutral state.

4. The control unit according to claim 1 wherein each control subunit proposes, based on a type of instruction to be executed, a possible state of its own to the arbitration block, and wherein only one of the plurality of control subunits will be in an active state, while the others in the plurality of control subunits are in a neutral state.

5. A method of designing a control unit that includes a microcontroller, the method comprising:

creating a functional description of an arbitration block structured to accept a plurality of inputs; and

creating a functional description of a plurality of individual control blocks, each control block having a first output coupled to a respective one of the plurality of

inputs of the arbitration block, and each control block having an input structured to accept a current state of the arbitration block.

6. The method of claim 5 wherein each of the plurality of individual control blocks also has a second output, the method further comprising:

creating a functional description of a collection block structured to accept a plurality of inputs structured to receive a respective signal from the second output of the plurality of individual control blocks, and the collection block structured to select one of the inputs as an output signal of the control unit.

7. The method of claim 5 wherein the control unit includes a finite state machine, and wherein the output of each of the plurality of control blocks is a proposed state.

8. The method of claim 5 wherein the output of each of the plurality of the individual control blocks does not directly couple to any of the other control blocks in the plurality of individual control blocks.

9. The method of claim 8 wherein each of the plurality of the individual control blocks is structured to receive the same current state of the arbitration block at the same time.

10. The method of claim 5 wherein creating a functional description of a plurality of individual control blocks comprises describing the functions of the plurality of individual control blocks in a hardware description language.

11. The method of claim 10 wherein describing the functions of the plurality of individual control blocks in a hardware description language comprises creating listing files in VHDL.

12. The method of claim 5 wherein each of the plurality of individual control blocks represents a separate class of instructions.

13. The method of claim 5 wherein each of the plurality of individual control blocks represents a separate class of operations.

14. The method of claim 5 wherein the control unit includes a microprocessor in place of the microcontroller.

15. A method of fabricating a control unit for electronic microcontrollers or microprocessors, the method comprising:

creating a finite state machine that further comprises:

creating a functional description of an arbitration block structured to accept a plurality of inputs; and

creating a function description of a plurality of individual control blocks that each correspond to a unique combinatorial logic circuit, each control block having a first output coupled to a respective one of the plurality of inputs of the arbitration block, and each control block having an input structured to accept a current state of the arbitration block.

16. The method of claim 15, wherein each of the plurality of individual control blocks is configured to include a second output, and the method further comprising:

creating a functional description of a collection block structured to accept a plurality of inputs structured to receive a respective signal from the second output of the plurality of individual control blocks, the collection block structured to select one of the inputs as an output signal of the control unit.

17. The method of claim 15, wherein creating a functional description of a collection block further includes structuring each collection block to output a proposed state.

18. The method of claim 15, wherein creating a functional description of a plurality of individual control blocks further comprises not directly coupling the output of each of the plurality of individual control blocks to any of the other control blocks in the plurality of individual control blocks.

19. The method of claim 18, wherein each of the individual control blocks is configured to receive the same current state of the arbitration block at the same time.

20. The method of claim 15, wherein creating a functional description of a plurality of individual control blocks comprises describing the functions of the plurality of individual control blocks in a hardware description language.

21. The method of claim 20, wherein describing the functions of the plurality of individual control blocks in a hardware description language comprises creating listing files in VHDL.

22. The method of claim 15, wherein each of the plurality of individual control blocks represents a separate class of instructions.